WHAT IS CLAIMED IS:

1. A method of varying the gain of an amplifier,

wherein the amplifier is comprised of an amplifier array and an automatic gain control (AGC) logic decoder,

wherein the amplifier array is further comprised of "n" amplifier circuit assemblies, where "n" is a positive integer, greater than 10,

wherein an "i^{th}" amplifier circuit assembly of the "n" amplifier circuit assemblies has an information input, a control input and one or more amplifier outputs, and

the AGC logic decoder is further comprised of "n" AGC amplifiers and "n" logic circuits,

wherein an i^{th} AGC amplifier of the "n" AGC amplifiers has two or more inputs and one or more outputs, each output being an AGC control signal, and

an i^{th} logic circuit of the "n" logic circuits has one or more logic inputs and one or more logic outputs, wherein a first logic output is an amplifier control signal and a second logic output is a shifting signal;

the method comprising the steps of:

(1) routing an AGC signal to a first input of the i^{th} AGC amplifier;

(2) comparing said AGC signal to an i^{th} scaled reference voltage, said i^{th} scaled reference voltage being received at a second input of the i^{th} AGC amplifier for all i between 1 and (n - q), inclusive, where q is a positive integer less than n;

(3) for all "i" between 1 and (n - q), inclusive, generating an i^{th} AGC control signal from the i^{th} AGC amplifier, wherein the i^{th} AGC control signal is a first logic level if said AGC signal is greater than said i^{th} scaled reference voltage, and is a second logic level if said AGC signal is less than said i^{th} scaled reference voltage;

(4) for all "i" between (n - q + 1) and "n", inclusive, generating an i^{th} AGC control signal from the i^{th} AGC amplifier, wherein the i^{th} AGC control signal is at said first logic level;

(5) routing said i^{th} AGC control signal to a first logic input of the i^{th} logic circuit;

(6) generating, in the i^{th} logic circuit, the i^{th} shifting signal;

(7) for all "i" between 1 and "m", inclusive, where "m" is a positive integer less than "n", routing the i^{th} shifting signal to a second logic input of the "j^{th}" logic circuit, where $j = i + p$ where p is a positive integer equal to (n - m);

(8) generating, in the i^{th} logic circuit, the i^{th} amplifier control signal, wherein the i^{th} amplifier control signal is a first control level when the i^{th} amplifier circuit assembly is to be turned "on", and is a second control level when the i^{th} amplifier circuit assembly is to be turned "off";

(9) routing the i^{th} amplifier control signal to the control input of the i^{th} amplifier circuit assembly;

(10) for all "i" between 1 and "p", inclusive, accepting, at the information input of the i^{th} amplifier circuit, an input signal;

(11) for all "i" between (p + 1) and "n", inclusive, accepting, at the information input of the i^{th} amplifier circuit, an i^{th} attenuated input signal;

(12) for all "i" between 1 and "p", inclusive, amplifying said input signal when the i^{th} amplifier control signal is at said first control level, thereby creating an i^{th} amplified signal;

(13) for all "i" between (p + 1) and "n", inclusive, amplifying said attenuated input signal when the i^{th} amplifier control signal is at said first control level, thereby creating an i^{th} amplified signal; and

(14) outputting, from the amplifier output of the i^{th} amplifier circuit, an i^{th} amplifier output signal, wherein said i^{th} amplifier output signal is said i^{th} amplified signal when the i^{th} amplifier control signal is at said first control level, and is a null signal when the i^{th} amplifier control signal is at said second control level.

2. The method of claim 1, further comprising the steps of:

(15) for all "i" between 1 and "n", inclusive, combining all said i^{th} amplifier output signals, thereby creating a combined amplified signal; and

(16) determining, from said combined amplified signal, said AGC signal.

3. The method of claim 2, further comprising the step of:

(17) demodulating said combined amplified signal.

4. The method of claim 1, wherein "n" is 35.

5. The method of claim 4, wherein "m" is 25 and "p" is 10.

6. The method of claim 4, wherein "q" is 3.

7. The method of claim 4, wherein "q" is 2.

8. The method of claim 4, wherein "q" is 1.

9. The method of claim 1, wherein said first logic level is a logic "1" and said second logic level is a logic "0".

10. The method of claim 1, wherein said first control level is a logic "1" and said second control level is a logic "0".

11. The method of claim 1, wherein said input signal is a cable TV signal.

12. The method of claim 1, wherein said input signal is routed to a resistor ladder, the resistor ladder having "m" nodes, wherein, for "i" between (p + 1) and

"n", inclusive, at an i^{th} node said input signal has been attenuated to be said i^{th} attenuated input signal.

13. A system for controlling the gain of an amplifier, comprising:

(a) a plurality of automatic gain control (AGC) amplifiers, a corresponding plurality of logic circuits, and a corresponding plurality of amplifier circuit assemblies; wherein:

(b) each of said plurality of AGC amplifiers has a first AGC input accepting an AGC signal; each of said plurality of AGC amplifiers has a second AGC input accepting a comparison signal; and each of said plurality of AGC amplifiers has an AGC output outputting an AGC control signal, said AGC control signal being at a first logic level when said AGC signal is equal to or greater than said corresponding comparison signal, and being at a second logic level when said AGC signal is less than said corresponding comparison signal,

(i) wherein, for AGC amplifier number 1 through AGC amplifier number (n - q), inclusive, said comparison signal is a scaled reference voltage wherein the scaled reference voltage at the i^{th} AGC amplifier is greater than the scaled reference voltage at the $(i + 1)^{th}$ AGC amplifier, where "n" is a positive integer greater than 10, and "q" is a positive integer less than "n", and

(ii) for AGC amplifier number (n - q + 1) through AGC amplifier number "n", inclusive, said comparison signal is an electrical ground;

(c) each of said plurality of logic circuits has a first logic input accepting said AGC control signal; logic circuit number (p + 1) through logic circuit number "n", inclusive, has a second logic input accepting an input logic shifting signal; each of said plurality of logic circuits has a first logic output outputting an output logic shifting signal, wherein said output logic shifting signal from logic circuit number 1 through logic circuit number (n - p), inclusive, is said input logic shifting signal for logic circuit number (p + 1) through logic circuit number "n", inclusive, respectively; and each of said plurality of logic circuits has a second logic output outputting an amplifier control signal, wherein

said amplifier control signal is at a first control level when said amplifier circuit assembly corresponding to said logic circuit is to be turned "on", and at a second control level when said amplifier circuit assembly corresponding to said logic circuit is to be turned "off", such that no more than "p" amplifier control signals are to be at said first control level at any time, wherein "p" is a positive integer less than "n";

(d) each of said plurality of amplifier circuit assemblies has a control input accepting a corresponding amplifier control signal; each of said plurality of amplifier circuit assemblies has a signal input, wherein, for amplifier circuit assembly number 1 through amplifier circuit assembly number "p", inclusive, said signal input accepts an information signal, and for amplifier circuit assembly number (p + 1) through amplifier circuit assembly number "n", inclusive, said signal input accepts an attenuated information signal, wherein attenuated information signal "i" is less attenuated than attenuated information signal (i + 1); and each of said plurality of amplifier circuit assemblies has an amplified output, wherein, for every amplifier circuit assembly receiving an amplifier control signal at said first control level, said amplifier output is an amplified signal, and for every amplifier circuit assembly receiving an amplifier control signal at said second control level, said amplifier output is a null signal; and

(e) each said amplified output is combined to form a combined amplified signal.

14. The system of claim 13, wherein said combined amplified signal is evaluated, thereby generating said AGC signal.

15. The system of claim 13, wherein said combined amplified signal is demodulated, creating a demodulated signal.

16. The system of claim 13, wherein "n" is equal to 35.

17. The system of claim 16, wherein "p" is equal to 10.

18. The system of claim 16, wherein "q" is equal to 3.

19. The system of claim 16, wherein "q" is equal to 2.

20. The system of claim 16, wherein "q" is equal to 1.

21. The system of claim 13, wherein said first logic level is a logic "1" and said second logic level is a logic "0".

22. The system of claim 13, wherein said first control level is a logic "1" and said second control level is a logic "0".

23. An amplifier array, comprising:

an input node;

a first set of amplifiers, arranged in a parallel fashion, and having their inputs tied together at said input node;

a resistor ladder coupled between said input node and ground; and

a second set of amplifiers, having their inputs tied to corresponding taps on said resistor ladder;

wherein outputs of said first set of amplifiers and outputs of said second set of amplifier are summed together at an output the amplifier array;

wherein gain for the amplifier array is adjusted by sequentially turning off one or more amplifiers in said first set of amplifiers, and sequentially turning on one or more amplifiers in said second set of amplifiers that correspond to said one or more amplifiers in said first set of amplifiers that are turned off.

24. The amplifier array of claim 23, wherein once all of said amplifiers in said first set of amplifiers are turned off, the gain of the amplifier array is further

adjusted by sequentially turning off one or more amplifiers in said second set of amplifiers.

25. The amplifier array of claim 23, further comprising at least one ferrite bead between coupled between said output of the amplifier array and a DC supply.

26. The amplifier array of claim 23, further comprising a capacitor coupled across one or more taps of said resistor ladder.

27. The amplifier array of claim 26, wherein said capacitor flattens the gain of said amplifier array over one or more attenuation settings.

28. The amplifier array of claim 23, further comprising a plurality of capacitors coupled across corresponding taps of said resistor ladder.

29. The amplifier array of claim 23, further comprising a plurality of comparators that correspond to each of said amplifiers in said first set of amplifiers and said second set of amplifiers, wherein each comparator compares a first voltage with a second voltage, resulting in a amplifier control signal that controls said corresponding amplifier in the amplifier array.

30. The amplifier array of claim 29, wherein said control signal turns on said corresponding amplifier when said first voltage is greater than said second voltage.

31. The amplifier array of claim 29, wherein said control signal turns off said corresponding amplifier when said second voltage is greater than said first voltage.

32. The amplifier array of 29, wherein said amplifier control signal causes said corresponding amplifier to operate linearly when a difference between said first voltage and said second voltage is less than a threshold.

33. The amplifier array of claim 29, further comprising a voltage divider having an input that receives an external automatic gain control voltage (AGC) having a voltage range, wherein said voltage divider compresses said voltage range of said AGC voltage to generate said first voltage .

34. The amplifier array of claim 33, wherein said voltage divider includes a means for adjusting compression of said external AGC voltage.

35. The amplifier array of claim 23, wherein said input node is single-ended.

36. The amplifier array of claim 23, wherein said output of the amplifier array is differential.

37. The amplifier array of claim 23, wherein said first set of amplifiers, said second set of amplifiers, are fabricated using one or more field effect transistors (FETs) process.

38. The amplifier array of claim 37, wherein said field effect transistors are fabricated using a CMOS process.

39. The amplifier array of claim 23, wherein said input node is coupled to a diplexer, and said output is coupled to a tuner.

40. The amplifier array of claim 23, further comprising at least one inductor coupled between said output and a DC supply.